REMARKS

This Amendment is in response to the Office Action mailed 09/01/2004. In the Office Action, the Examiner rejected claims 1-25 under 35 U.S.C. § 103. Reconsideration in light of the amendments and remarks made herein is respectfully requested.

Rejection Under 35 U.S.C. § 103

3. The Examiner rejects claims 1-2, 6-7, 11-12, and 21-22 under 35 U.S.C. § 103(a) as being unpatentable over Isaka (US 6,654,455) in view of Iwama et al. (US 6,600,735).

As to claim 1, the Examiner asserts that Isaka teaches sending a voice packet related to the voice data to the line card without duplication. Applicant understands Isaka to teach that packetized voice signals are duplicated and sent to all telephones participating in a conference except for the phone that originated the voice signal. Col. 8, lines 64-66.

The Examiner asserts that Isaka teaches selectively multicasting the voice data stored in the memory to the plurality of user devices based on the descriptor fields in the voice packet, citing a CPU included in a telephone that identifies a packet meant for the telephone. Applicant respectfully submits that the Examiner has not fully considered the elements as claimed. As claimed, the user devices all interface to a single line card which is not how the telephones taught by Isaka are configured. The voice packet is sent to the line card without duplication. Therefore the one instance of voice data stored in the memory is multicast to the plurality of user devices based on the one voice packet sent to the line card. This is entirely unlike the way of sending packetized voice data to a plurality of telephones taught by Isaka which does not store voice data in a memory and does not control the multicasting of the stored voice data to a plurality of user devices with an unduplicated voice packet.

The Examiner admits that Isaka fails to teach storing the voice data in a memory. The Examiner asserts that Iwama teaches storing voice data in a memory citing a storage device 1802 in Figure 9. Iwama teaches a method for managing communication bandwidth. Iwama teaches that the storage device is for storing indexes representing the performance of the network. Col. 14, lines 54-64. Nothing in Iwama teaches or suggests storing voice data as claimed.

The Examiner asserts that one would have been motivated to modify Isaka to monitor communication quality under bandwidth reservation. Nothing in Isaka teaches or suggests a requirement for bandwidth reservation. Applicant respectfully submits that monitoring communication quality under bandwidth reservation does not provide a motivation to combine the references because bandwidth reservation is unrelated to the teachings of Isaka. In any event, even if Isaka was modified to introduce the memory of Iwama, the resulting system would still not store voice data in the memory as now claimed.

As to claim 2, applicant relies on the patentability of the claims from which this claim depends to traverse the rejection without prejudice to any further basis for patentability of this claim based on the additional elements recited.

As to claims 6-7, 11-12, and 21-22, the Examiner asserts that these claims do not teach or define any new element above claims 1-2 and the Examiner rejects these claims for similar reasons as claims 1-2. Applicant likewise traverses the rejections for similar reasons.

Applicant respectfully requests that the Examiner withdraw the rejection of claims 1-2, 6-7, 11-12, and 21-22 under 35 U.S.C. § 103(a) as being unpatentable over Isaka in view of Iwama.

4. The Examiner rejects claims 3, 8, 13, 19, and 23 under 35 U.S.C. § 103(a) as being unpatentable over Isaka (US 6,654,455) in view of Iwama et al. (US 6,600,735), and further in view of Onishi et al. (US 5,434,863).

As to claim 3, the Examiner admits that Isaka fails to teach the method of claim 1, wherein the descriptor fields include a memory pointer field, status field, mask field, or a data length field. The Examiner asserts that Onishi teaches the descriptor fields include a memory pointer field, status field, mask field, or a data length field citing a field 401 of an IP address for representing the destination network and subnet mask data 402 for representing subnet information of the destination network. Applicant respectfully submits that neither of these fields taught by Onishi is a memory pointer field, status field, mask field, or a data length field as those terms are defined by paragraphs [0029] and [0030] of the specification.

As to claims 8, 13, 19, and 23, the Examiner asserts that these claims do not teach or define any new element above claims 1-2 and the Examiner rejects these claims for similar reasons as claim 3. Applicant likewise traverses the rejections for similar reasons.

Applicant respectfully requests that the Examiner withdraw the rejection of claims 3, 8, 13, 19, and 23 under 35 U.S.C. § 103(a) as being unpatentable over Isaka in view of Iwama, and further in view of Onishi.

5. The Examiner rejects claims 4-5, 9-10, 14, and 24-25 under 35 U.S.C. § 103(a) as being unpatentable over Isaka (US 6,654,455) in view of Iwama et al. (US 6,600,735), in view of Onishi et al. (US 5,434,863), and further in view of Lin et al. (US 6,651,225).

As to claim 4, the Examiner admits that Isaka fails to teach using a multicast hardware accelerator to send the voice data to selected user devices based on the mask field. The Examiner asserts that Lin teaches a hardware accelerator citing item 120 of Figure 2. Lin teaches a dynamic logic evaluation system. Applicant respectfully submits that Lin is non-analogous art and that one of ordinary skill in the art would not be motivated to consider the teachings of Lin in connection with voice communication.

The hardware accelerator taught by Lin is a modeling of a circuit design where the model is implemented in hardware, such as a FPGA. The hardware model is used as an alternative to software simulation for portions of the cycles being modeled for the circuit design. Col. 15, line 57, through Col. 19, line 14. Nothing in Lin teaches or suggests "a multicast hardware accelerator to multicast the voice data stored in the buffer memory to ports selected from the plurality of ports by a single voice packet received from the host system" as now claimed.

The Examiner asserts that one would have been motivated to modify Isaka to provide the hardware accelerator of Lin to allow multiple users doing interactive operations in a manner that allows each user to shift back and forth between hardware emulation and software simulation to discover and eliminate problems in the IC design. Applicant respectfully points out that Isaka provides an IP conference telephone system and has nothing to do with IC design or emulation or simulation thereof. There is no motivation to apply the teachings of Lin to Isaka based on the benefits set forth by the Examiner because these benefits relate to the modeling of a circuit design and have no relation at all to IP communications.

As to claim 5, applicant relies on the patentability of the claims from which this claim depends to traverse the rejection without prejudice to any further basis for patentability of this claim based on the additional elements recited.

As to claims 9-10, 14, and 24-25, the Examiner asserts that these claims do not teach or define any new element above claims 1-2 and the Examiner rejects these claims for similar reasons as claim 3. Applicant likewise traverses the rejections for similar reasons.

Applicant respectfully requests that the Examiner withdraw the rejection of claims 4-5, 9-10, 14, and 24-25 under 35 U.S.C. § 103(a) as being unpatentable over Isaka in view of Iwama, in view of Onishi, and further in view of Lin.

6. The Examiner rejects claims 16-18 and 20 under 35 U.S.C. § 103(a) as being unpatentable over Isaka (US 6,654,455) in view of Iwama et al. (US 6,600,735), and further in view of Lin et al. (US 6,651,225).

As to claim 16, the Examiner asserts that Isaka teaches a host system and a line card. The Examiner admits that Isaka does not teach a buffer memory. The Examiner asserts that Iwama teaches a buffer memory and that it would have been obvious to combine the teachings of Isaka and Iwama to achieve the claimed device. The Examiner admits that Isaka does not teach a multicast hardware accelerator. The Examiner asserts that Lin teaches a hardware accelerator and that it would have been obvious to combine the teachings of Isaka, Iwama, and Lin to achieve the claimed device.

Applicant has amended claim 16 to more clearly distinguish the claimed invention from the teachings of Isaka, Iwama, and Lin.

The Examiner reads the claimed element of a host system on the multicast router 70 taught by Isaka. The Examiner asserts that Isaka teaches a line card citing the teaching of at least three telephone terminal systems connected to a conference trunk, the multicast router 70 being substituted for the conference trunk 24, and a CPU 40 included in each of the telephone terminal systems identifying a packet meant for the telephone. Col. 7, lines 26-32, and 60-65. The Examiner appears not to consider that what is claimed is a network device that includes the claimed elements. The Examiner has cited element taught by Isaka that are distributed and coupled by an IP network. Applicant respectfully submits that Isaka does not teach or suggest these elements comprising a single network device as claimed. To more clearly point out and claim the network device, applicant has amended the claim to include elements of inter-relationship and cooperation between the host system, the line card, and a buffer memory. As

amended it is clear that the line card is able to multicast voice data stored in the buffer memory to a plurality of ports provided by the line card as selected by a single voice packet received from the host system. Isaka teaches a system where a conference trunk adds and subtracts packetized voice signals from a plurality of telephones in an IP-PBX to allow a conference between telephones in the IP-PBX. Nothing in Isaka teaches or suggests that the host system causes the line card to multicast to its ports responsive to a single voice packet provided by the host system.

The Examiner admits that Isaka does not teach a buffer memory. The Examiner asserts that Iwama teaches a buffer memory citing a storage device 1802 in Figure 9. Iwama teaches a method for managing communication bandwidth. Iwama teaches that the storage device is for storing indexes representing the performance of the network. Col. 14, lines 54-64. Nothing in Iwama teaches or suggests storing voice data extracted from the network packet by the host system as now claimed.

The Examiner asserts that one would have been motivated to modify Isaka to introduce the buffer of Iwama to retain information as close to the input/output loop as possible to reduce access time. Applicant fails to see where such a motivation to combine the references is found in either of the references. Further, one would expect that buffering would increase the access time as compared to the unbuffered system taught by Isaka. In any event, even if Isaka was modified to introduce the buffer of Iwama, the resulting system would still not provide a buffer memory as now claimed.

The Examiner admits that Isaka does not teach a multicast hardware accelerator. The Examiner asserts that Lin teaches a hardware accelerator citing item 120 of Figure 2. Lin teaches a dynamic logic evaluation system. Applicant respectfully submits that Lin is non-

analogous art and that one of ordinary skill in the art would not be motivated to consider the teachings of Lin in connection with voice communication.

The hardware accelerator taught by Lin is a modeling of a circuit design where the model is implemented in hardware, such as a FPGA. The hardware model is used as an alternative to software simulation for portions of the cycles being modeled for the circuit design. Col. 15, line 57, through Col. 19, line 14. Nothing in Lin teaches or suggests "a multicast hardware accelerator to multicast the voice data stored in the buffer memory to ports selected from the plurality of ports by a single voice packet received from the host system" as now claimed.

The Examiner asserts that one would have been motivated to modify Isaka to provide the hardware accelerator of Lin to allow multiple users doing interactive operations in a manner that allows each user to shift back and forth between hardware emulation and software simulation to discover and eliminate problems in the IC design. Applicant respectfully points out that Isaka provides an IP conference telephone system and has nothing to do with IC design or emulation or simulation thereof. There is no motivation to apply the teachings of Lin to Isaka based on the benefits set forth by the Examiner because these benefits relate to the modeling of a circuit design and have no relation at all to IP communications.

As to claim 17, applicant relies on the patentability of the claims from which this claim depends to traverse the rejection without prejudice to any further basis for patentability of this claim based on the additional elements recited.

As to claim 18, the Examiner asserts that Isaka teaches the host system is to send a packet relating to the data stored in the buffer memory, the packet includes descriptor fields used to multicast the data stored in the buffer memory. Applicant has amended claim 18 in view of the amendments to claim 16. Since the Examiner has admitted that Isaka fails to teach a buffer

memory in connection with claim 16, applicant fails to understand how Isaka can disclose a packet to multicast data stored in a buffer memory. The portions of Isaka cited by the Examiner appear merely to describe that packets including voice data are sent to an IP network where a CPU in an attached telephone identifies those packets meant for the telephone. This does not disclose a voice packet that enables multicasting of voice data that is stored in a buffer memory as now claimed.

As to claim 20, applicant has cancelled the claim.

Applicant respectfully requests that the Examiner withdraw the rejection of claims 16-18 and 20 under 35 U.S.C. § 103(a) as being unpatentable over Isaka in view of Iwama, and further in view of Lin.

Conclusion

Applicant respectfully requests that a timely Notice of Allowance be issued in this case.

Respectfully submitted,

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By _____

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